**EAST WEST UNIVERSITY**

**Department of Computer Science and Engineering  
  
Semester:** Spring 2017  
**Course Number:** CSE345  
**Course Title:** Digital Logic Design

**Experiment Number:** 01  
**Experiment Title:** Schematic and Structural Verilog Simulation of Combination Logic Circuits

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**Student ID:** 2014-1-60-032

**Group Number:** 01  
**Group IDs:**

2014-1-60-032  
2015-1-60-065  
2015-1-60-071  
2015-1-60-081  
  
**Date of Performance:   
Date of Report Submission:**

**Objectives:**

1. To learn schematic simulation of combination logic circuits using Quartus II software.

2. To learn structure Verilog simulation of combination logic circuits using Quartus II software.

**Answers to the Pre-Lab Questions:**

1. The function derived from the logic diagram

S=A'B'C + A'BC' + AB'C' + ABC

**Truth Table**

|  |  |
| --- | --- |
| ABC | S |
| 000 | 0 |
| 001 | 1 |
| 010 | 1 |
| 011 | 0 |
| 100 | 1 |
| 101 | 0 |
| 110 | 0 |
| 111 | 1 |

**2.Verilog code:**

module expt(input A,B,C,

output S);

wire w1 , w2 ,w3 ,w4;

and g1 (w1, ~A, ~B, C),

g2 (w2, ~A, B, ~C),

g3 (w3, A, ~B, ~C),

g4 (w4, A, B ,C);

or g5 (S, w1, w2, w3, w4);

endmodule